SIEMENS

SIMATIC S5

342 Parity check module

6ES5 342-3AA11

Instructions

Ord. No. C79000-B8576-C245-3

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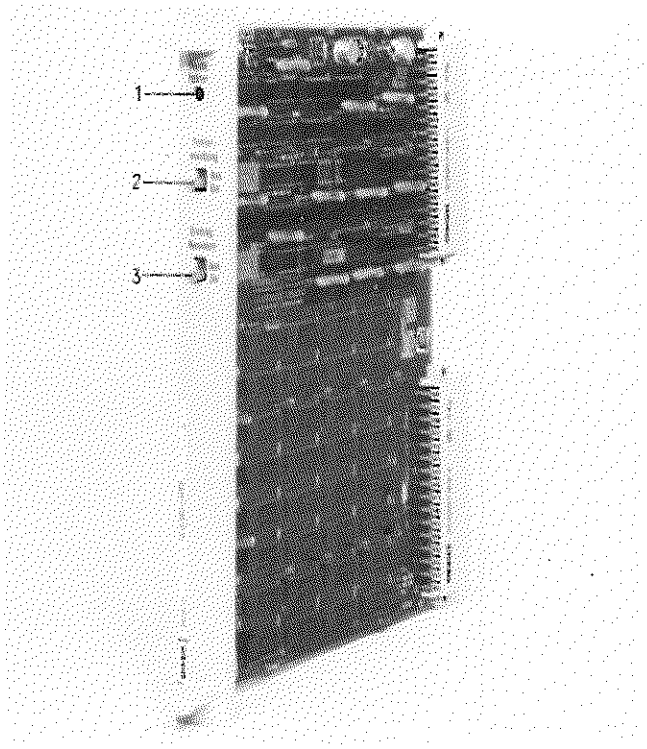

1 „Parityfehler" LED (parity error)
2 „Fehlermeldung" switch (error indication)
3 „Eintrag Neustart" switch (cold restart)

1 Technical description

1.1 Application

The 342 parity check module is required in the PC 150 S programmable controller for monitoring the main memory or the 340/350 external memory.

1.2 Construction

The module is constructed as a plug-in printed circuit board.

Two switches for selecting the operating mode and a red LED for displaying a parity error are incorporated in the front panel (Fig. 1).

1.3 Principle of operation

- **Parity generation**

  The parity module reads the data during read and write sequences on the bus. Two parity bits are generated during the write sequence from each data (one parity bit per byte) and deposited in a memory (RAM, buffered) under the address, available on the bus.

- **Parity comparison**

  The two output bits from the parity generator are compared with the stored bits from the RAM during the read sequence on the bus, in a non-inhibited area.

- **Error address register**

  If a fault condition is available, the address of the erroneous data is accepted in the readable register, a red LED is set on the front panel and a signal of 200 ms is outputted to the CPU.

Monitored memory areas

- **Main memory**

  The parity monitoring covers the following ranges:

  $8 \cdot 2^{10}$ to $56 \cdot 2^{10}$,
  $58 \cdot 2^{10}$ to $59¼ \cdot 2^{10}$ and
  $59½ \cdot 2^{10}$ to $60 \cdot 2^{10}$.

- **External memory**

  The parity monitoring covers the full range from 0 to $64 \cdot 2^{10} - 1$. The monitored address range is switched-over via a slot identification.

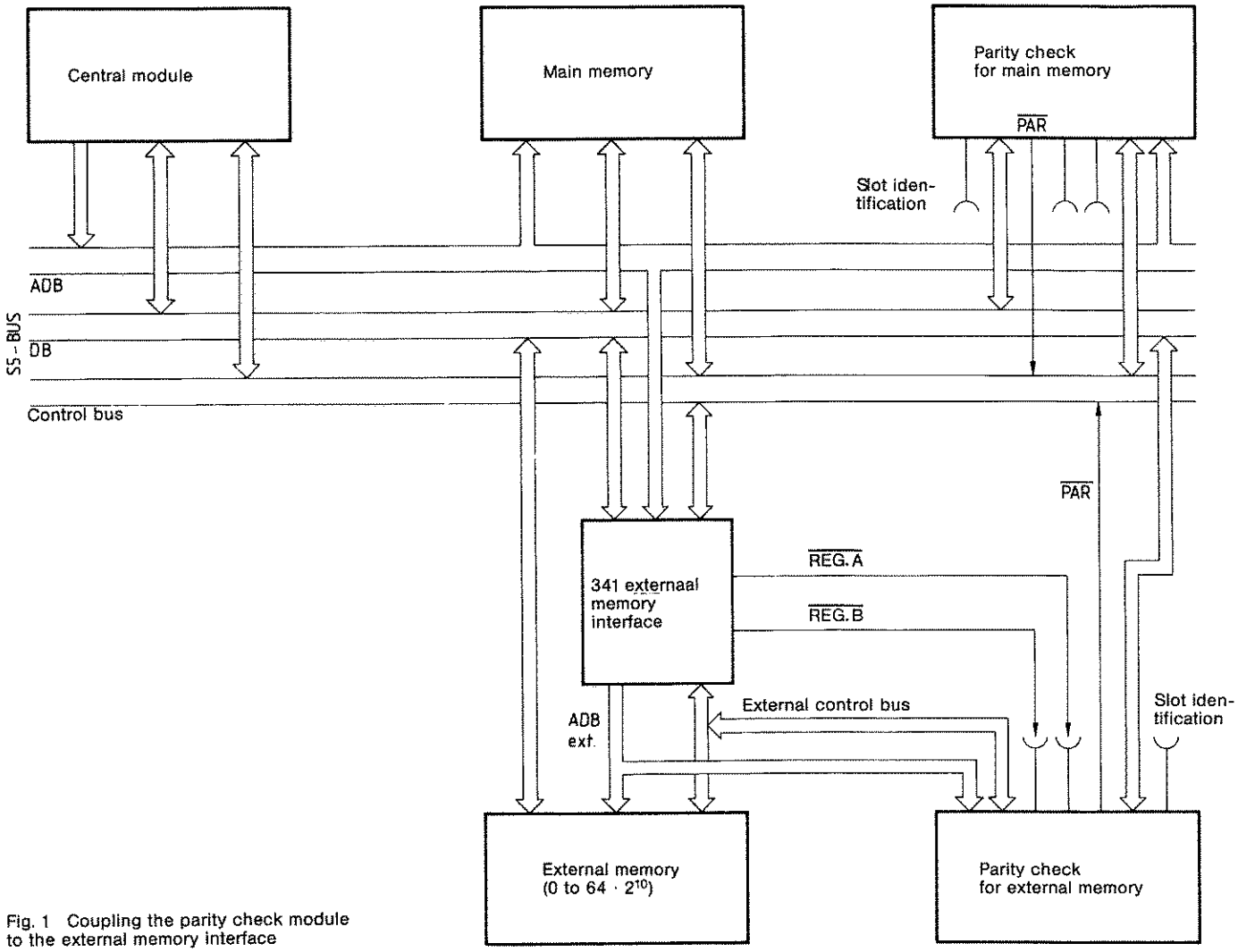

Fig. 1 Coupling the parity check module to the external memory interface

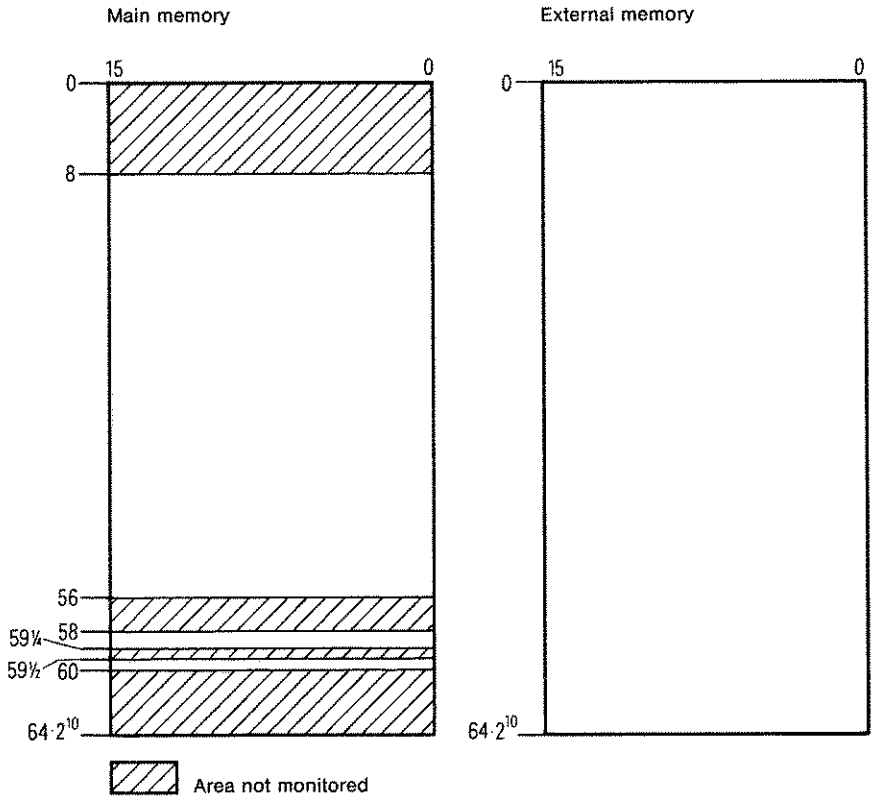

Fig. 3 Monitored memory areas

1.4 Technical data

Supply voltage	5 V ± 5%
Buffer voltage	3.8 to 4.75 V
Current consumption during operation during buffering [1]	 1.5 A 10 µA
Access time	450 ns between the negative and positive going edges of MEMR/MEMW
Permissible ambient temperature during operation during storage and transport	 0 to 55 °C -40 to 70 °C
Humidity rating	95% relative humidity at 25 °C
Operating altitude	up to 3000 m above sea level
Dimensions (W x H x D)	20 mm x 244 mm x 195 mm
Weight	approx. 0.3 kg

[1] During buffer operation, the voltage available on the 5-V supply line must be lower than +0.8 V in order to obtain the specific buffer current.

1.5 Jumper assignment

The underlined meanings indicate the condition as supplied.

Location X3	Meaning open	Meaning closed
1–16	2 parity bits/words	1 parity bit/word
2–15	1 parity bit/word	2 parity bits/words
3–14	1 parity bit/word	2 parity bits/words
4–13	2 parity bits/words	1 parity bit/word
5–12	Test	Operation
6–11	Test	Operation
7–10	Test	Operation
8– 9	Test	Operation

Location X4	Meaning open	Meaning closed
1–16	External memory completely monitored	External memory only partially monitored
2–15	Main memory completely monitored	Main memory only partially monitored
3–14	Test	Operation
4–13	Not occupied	Not occupied
5–12	Test point pin 5	Test point pin 5
6–11	Test point pin 6	Test point pin 11
7–10	Not occupied	Not occupied
8– 9	Test point pin 8	Test point pin 8

Attention: Either 1–16 or 2–15 can be inserted in location X4.

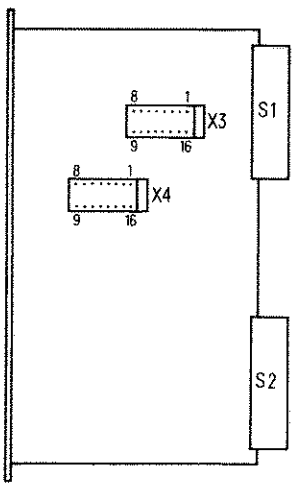

Fig. 4 Jumper mounting positions

2 Mounting

The module is withdrawn towards the front by making light up and down movements on the withdrawing handle. The module may only be withdrawn or inserted, when the central controller, the extension units and the transmitter units are switched off. Faults can occur if this is not adhered to. The buffering is also interrupted when the module is withdrawn. The RAM data is lost.

A parity generation must be made when setting-up the module.

The parity module is used for monitoring the main memory and the external memory. The monitored area is switched-over using the slot identification (refer to the PC 150 S operating instructions).

3 Operating and display elements

Switch		Function	
S2 „Eintrag Neustart"	S1 „Fehler-meldung"	Parity generation at cold re-start	Error indication and LED display
off	off	no	no
off	on	no	yes
on	off	yes	no
on	on	yes	yes

Aus = off
Ein = on

4 Interface assignment

Base connecter 1

	d	b	z
2	UBATT	0 V	+5 V
4			
6	ADB 12	ADB 0	CPKL
8	ADB 13	ADB 1	$\overline{\text{MEMR}}$
10	ADB 14	ADB 2	$\overline{\text{MEMW}}$
12	ADB 15	ADB 3	$\overline{\text{RDY}}$
14		ADB 4	DB 0
16		ADB 5	DB 1
18		ADB 6	DB 2
20		ADB 7	DB 3
22		ADB 8	DB 4
24		ADB 9	DB 5
26		ADB 10	DB 6
28	$\overline{\text{DS}}$	ADB 11	DB 7
30			
32		0 V	

Base connector 2

	d	b	z
2		0 V	+5 V
4		DB 8	DB 12
6		DB 9	DB 13
8		DB 10	DB 14
10		DB 11	DB 15
12			
14			
16			
18			
20			
22			
24		Slot identification	
26		PAR	
28		$\overline{\text{REG. A}}$	
30		$\overline{\text{REG. B}}$	
32		0 V	

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