SIEMENS

SIMATIC S5

S5-150 U Central Controller

6ES5150-3SB61

Instructions

Order No. C79000-B8576-C346-02

Contents

1 Description

1.1 Application

The SIMATIC S5-150 U programmable controller is a variant of the most powerful central controller in the S5 family, the SIMATIC S5-150 S.

The entire STEP 5 operation set can execute on this PC. This makes the S5-150 U suitable for complex control applications, as well as for closed-loop control and listing tasks.

The possibility of configuring either with the 512 interface module or the new communications processors, such as the CP 524, CP 525, CP 526 and CP 535, makes a wide spectrum of operator communication and monitoring and communication facilities available.

1.2 Construction

The S5-150 U is a self-contained subrack. A central controller expansion unit, such as that of the S5-150 S, is not required. The external memory is situated in the central controller to the left of the CPUs. For applications where the number of slots for communications processors is insufficient, an expansion unit is available with the necessary interface modules, in which digital and analog I/Os, CPs and intelligent I/Os can be operated (the 185 expansion unit with the IM 304/IM 314 interface modules).

The power supply unit is in the base of the central controller (primary 220 V/115 V, secondary 5 V/40 A, 24 V and 15 V optionally). Power supply and fan operate at the same voltage.

The subrack has the same compact design as the 135 U PC and the 183 U expansion unit.

Possible configurations

The 924 S, 925 S, 926 S and 927 S CPUs are assigned to slots 35, 43, 51 and 59 respectively. Of the 16 remaining slots, 5/6 can be operated in two different versions by modifying the interfaces.

The following table shows all possible configurations:

Slot	3	11	19	27	69	79	89	99	107	115	123	131	139	147	155	163
Module																
PG interface 6ES5 511–5AA12																
340 memory 6ES5 340–3K...																
350 memory 6ES5 350–3KA..																
302 EU interface 6ES5 302–3KA..																
300 EU interface 6ES5 300–5CA..																
300 EU interface 6ES5 300–3AB..																
301 EU interface 6ES5 301–5CA..																
301 EU interface 6ES5 301–3AB..																
512C (G/E) interface 6ES5 512–5BC..																
CP 6ES5 5..–....																
Jumpering card 6ES5 756–0AA11																

EU = Expansion unit

Table 1 Complement as delivered

The soldered jumpers 1 to 11 are on the solder side of the wiring backplane and are easily accessible if the back of the PC is removed.

Jumpers 1 to 11 are all open.

Module \ Slot	3	11	19	27	69	79	89	99	107	115	123	131	139	147	155	163
External memory interface 6ES5 341-4AA11																
340/350 memory 6ES5 340/6ES5 350																
Parity module 6ES5 342-3AA11		BR11							BR9	BR10						
CP 6ES5 5..-.....													BR1...8			

Table 2 Possible conversions

BR = Jumper

The soldered jumpers 1 to 11 are on the solder side of the wiring backplane and are easily accessible if the back of the PC is removed.

The jumpers specified must be inserted.

	163	156	147	139	131	123	115	107	99	89	79	69	59	51	43	35	27	19	11	3
	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ
2																				
4				BR1																
6				[]																
8																				
10																				
12																				
14																				
16																				
18																				
20																				
22																				
24					BR5															
26					[]															
28																				
30																				
32																				
						C79040-A32-C652-88															
					+24V-															
	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ	DBZ
2																				
4																				
6																				
8																				
10					BR7															
12					[]															
14																				
16					BR8															
18					[]															
20																				
22					BR6															
24					[]															
26								BR10	BR9											BR11
28		BR3	BR2	BR4				[]	[]											[]
30		[]	[]	[]																
32																				

Explanation

- Slots 3 to 27

If the jumpering card is plugged into slot 27 and if jumper 11 is not inserted, slots 3, 11 and 19 are suitable for CP 5xx modules (configuration as delivered).

If the external memory interface module is inserted in slot 27, slots 3, 11 and 19 are configured for 340/350 memory modules used as external memories. If jumper 11 is soldered in, slot 3 is wired for the external memory parity module.

- Slots 107, 115

As delivered (jumpers 9 and 10 not inserted) the CP 5xx, 302 interface module or the 340/350 memory modules can be used in both slots as desired.

If jumper 9 is soldered in, slot 107 is configured for the parity module. If jumper 10 is soldered in, slot 115 is configured for the parity module.

- Slots 139, 147

As delivered (jumpers 1 to 8 not inserted), the two slots are configured for the 301 expansion unit interface module (compact version) or the 302 expansion unit interface module.

If jumpers 1 to 8 are soldered in, the two slots are configured for the CP 5xx.

1.3 DMA priority assignment

The CP 5xx modules do not use DMA (direct memory access) for accessing the main memory. They have dual-port RAMs, which are fed via manipulation blocks (diskette with FBs: 6ES5844-0CA11).

For operating the 511 interface module and one pair of 512 modules, the DMA circuit has been retained in the PC.

The following priority assignment applies:

Slot	69	79	89	99
Module	511 IM	511 IM	512 IM G	512 IM E
Priority	1	2	3	
Slot identification code (binary)	000	001	010	

If the 512 module is to be used, slot 79 must be occupied.

Operation with the 512 and CP 5xx

The S5-150 U can be operated only with 512 modules or only with CP 5xx modules and the respective function blocks.

If the 512 and CP 5xx are used together, care must be taken that the interface data address area is not doubly addressed. For this, interfaces 0 to 3 must be assigned to 512 modules and interfaces 4 to 15 must be kept free.

If the CP 535 or the Ethernet bus interface for SINEC H1 is to be used, a power supply module for supplying 15 V to the CP slots must be built into the power supply chassis. Its Order No. is 6ES5 956-0AA11.

1.4 Principle of operation

1.4.1 Schematic of the central processor

The **byte processor** performs arithmetic and word operations. The processing width is 8, 16 or 24 bits.

The **bit processor** includes a logic unit, which performs Boolean logic operations, as well as executing sophisticated bit check instructions. Logic processing is possible up to 7 bracket levels.

The **I/O register** is used for temporarily storing the data during I/O transfer.

The **address processor** generates the addresses for memory accesses, e.g. to the flag area, input area, and for opcode-fetch sequences.

The **clock generator** produces control signals for I/O control, memory access, as well as the basic clock.

The **interrupt controller** detects hardware and software errors, such as NAU (powerfail), BAU (battery low) or QVZ (time-out).

The **opcode decoder** generates a microprogram starting address for each statement.

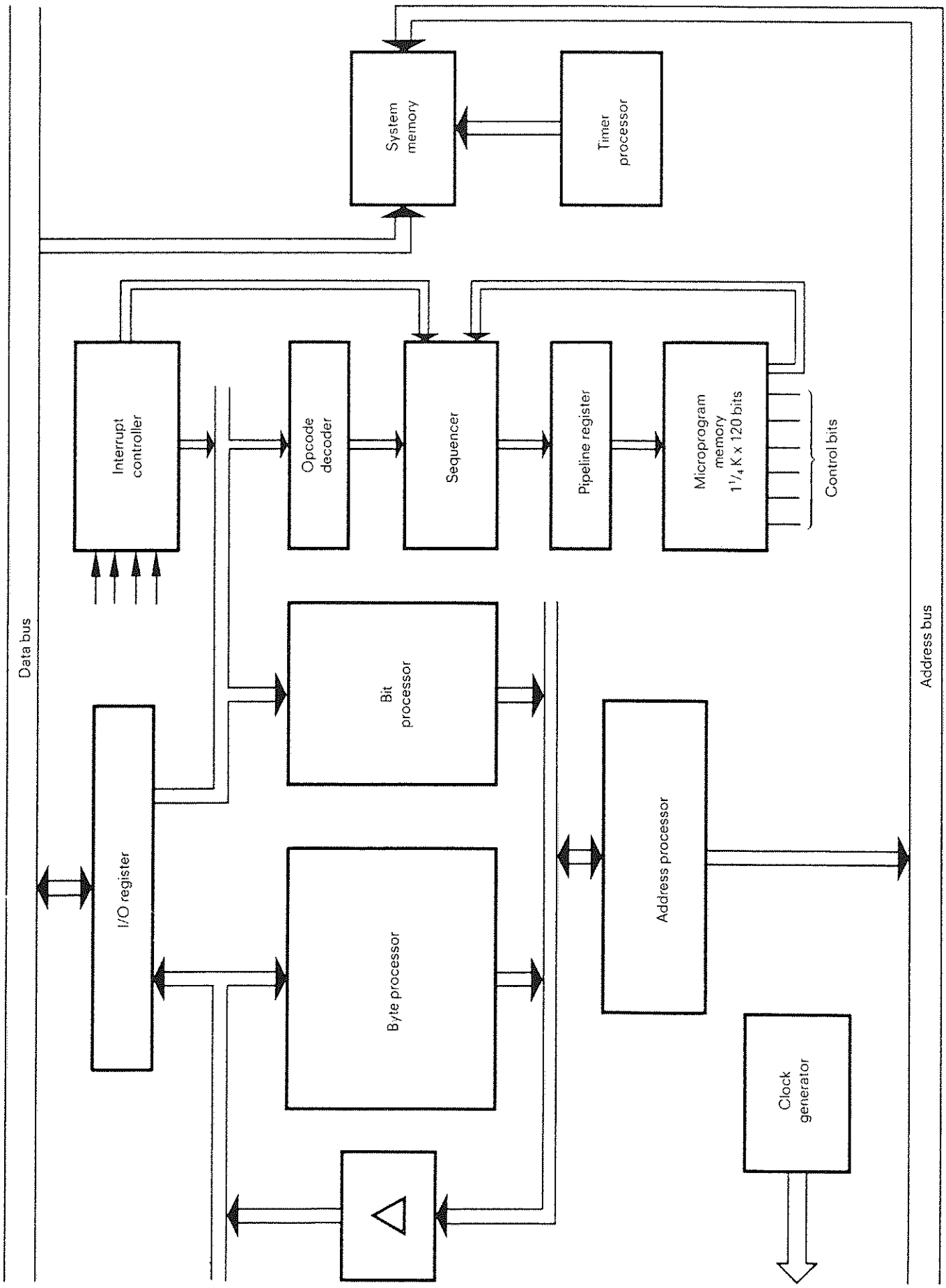
The **sequencer** controls the necessary microaddresses for the microprogrammed CPU.

The **pipeline register** decouples the current address of a micro-instruction from the generation of the subsequent microinstruction address.

The **microprogram memory** contains the control information for all hardware components in the central processor ($1^1/_4$ K micro-words, each 120 bits long).

The **system memory** contains the data for the operating system, the process image for digital inputs and outputs, flags, counters, timers and the system software.

The **timer processor** updates the relevant timer locations on a defined time base (0.01 s, 0.1 s, 1 s, 10 s), thus off-loading the byte processor. The processor accesses the timer locations via a separate bus.

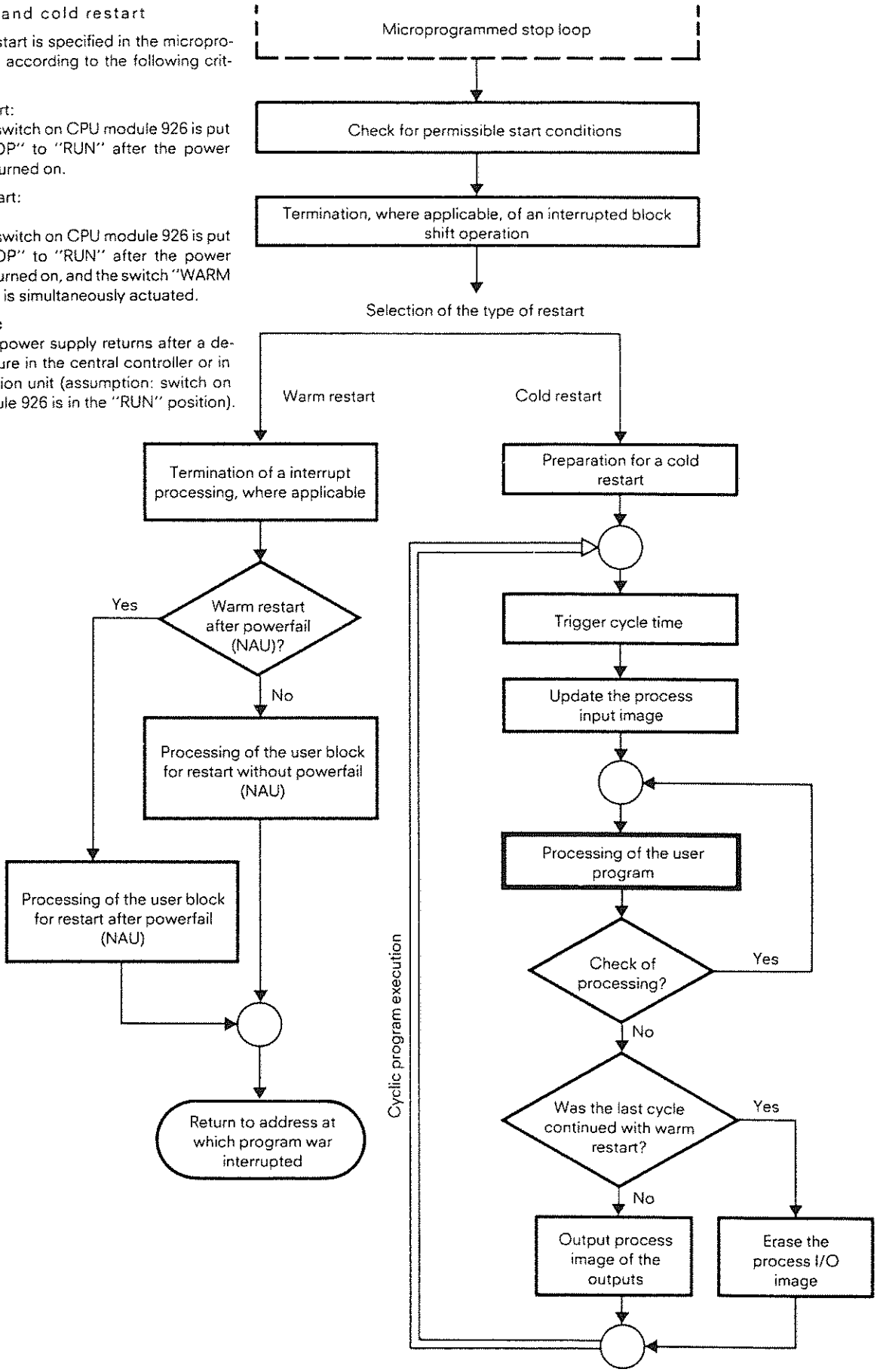

System memory
Timer processor
Interrupt controller
Opcode decoder
Sequencer
Pipeline register
Microprogram memory 1¼ K x 120 bits
Control bits
Data bus
Address bus
Bit processor
I/O register
Byte processor
Address processor
Clock generator

1.4.2 Warm and cold restart

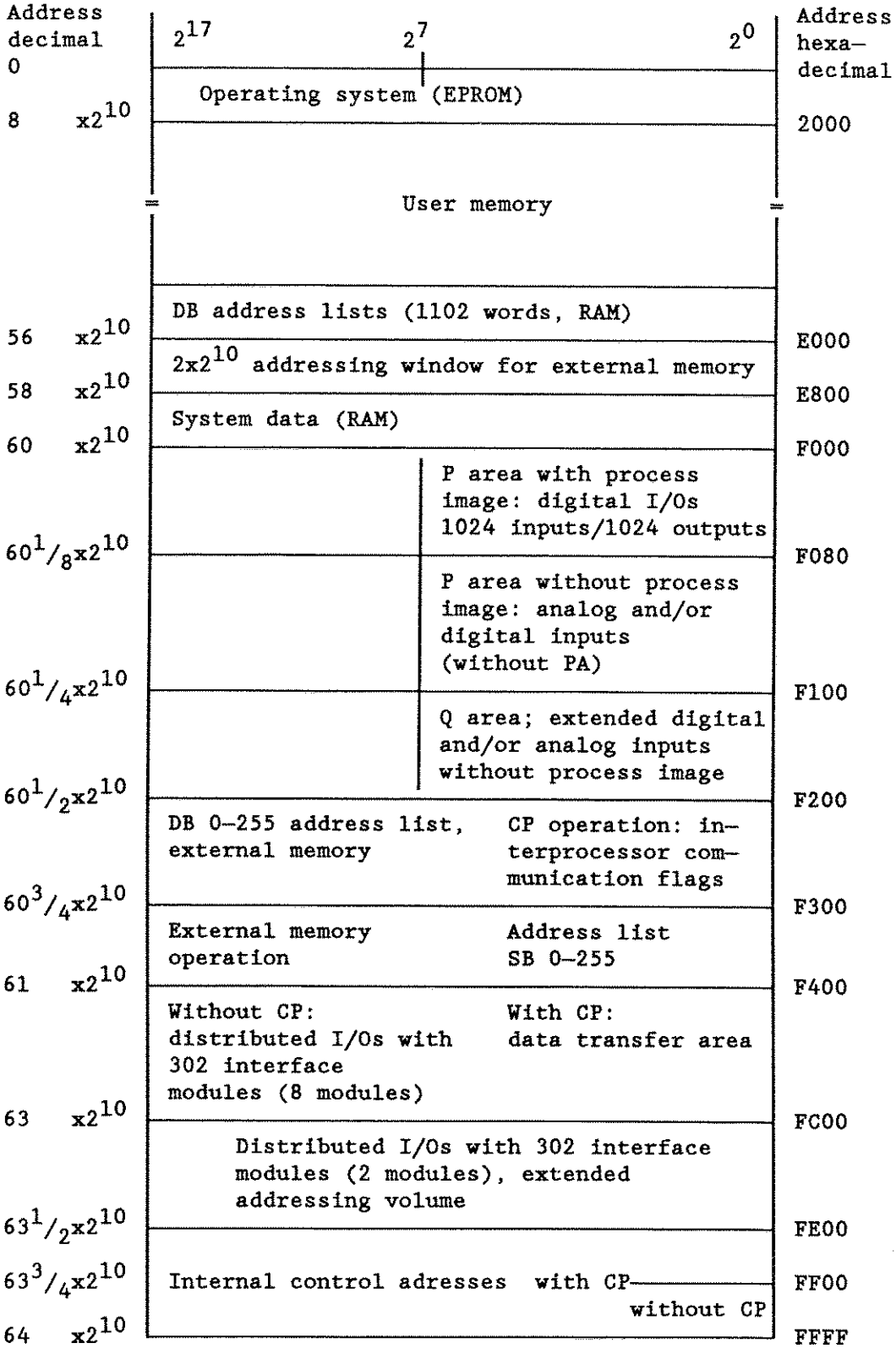
The type of restart is specified in the microprogrammed loop according to the following criteria:

- Cold restart:
  When the switch on CPU module 926 is put from "STOP" to "RUN" after the power has been turned on.
- Warm restart:
  Manual
  When the switch on CPU module 926 is put from "STOP" to "RUN" after the power has been turned on, and the switch "WARM RESTART" is simultaneously actuated.

  Automatic
  When the power supply returns after a detected failure in the central controller or in the extension unit (assumption: switch on CPU module 926 is in the "RUN" position).



1.5 Memory map



The external memory address list and the interprocessor communication flags for the CPs occupy the same area. This means that, if the external memory and CPs are used together, the interprocessor communication flags must be fully disabled (jumper setting) and that their function is not available. The interprocessor communication flags can be indirectly accessed with the LIR and TIR STEP 5 operations.

The data transfer area of the CPs and most of the address area for serially linked distributed I/Os occupy the same address area, i.e. if CPs are used, only two 302 interface modules can be operated simultaneously for distributed I/Os and they must have the starting addresses OFC00H (63×2^{10}) and OFD00H ($63^{1}/_{4} \times 2^{10}$).

The internal control address area is free for an AS 302 interface module with distributed I/Os (OFE00H $63^{1}/_{2} \times 2^{10}$) as a CP is not used.

Digital and analog I/O modules cannot be used together.

1.6 Technical specification

Permissible ambient temperature	
Operation	0 to 55 °C (32 to 131 °F)
Storage and transport	-40 to 70 °C (-40 to 158 °F)
Humidity rating	F to DIN 40040 (95 % relative atmospheric humidity at 25 °C (77 °F), no condensation)
Degree of protection to DIN 40050 and IEC 144	IP00 (no protection)
Insulation class	B to VDE 0110
Galvanic isolation, primary/ secondary	to VDE 0805
Operating altitude	up to 3500 m (11,500 ft.) above sea-level
Mechanical requirements	Installation in fixed equipment, not necessarily free of vibrations; installation on board ships and in motor vehicles if the relevant regulations are observed, but not directly mounted on the engine assembly.
Socket connector	to DIN 41612, Part 3
Dimensions	to DIN 41494, Part 1
Internal supply voltage	5 V ±5 %
Current consumption of the central processing modules	12.7 A (typical)
Current consumption in back-up operation	max. 0.28 mA
Execution times [1]	
Logic operations	2 µs
2^{10} mixed operations [2]	< 3 µs

Maximum number of	
digital inputs [3]	1024 with process image 1024 without process image
digital outputs [3]	1024 with process image 1024 without process image
Flags (internal relays)	2048, retentive
Data blocks PB, FB, SB, OB	256, each with 256 words
Timers	256, retentive (0.01 to 9990 s)
Counters	256 (0 to 999)
Analog input channels [3]	192
Analog output channels [3]	192
Maximum memory configuration	
main memory	48 x 2^{10} (16 bits wide), RAM and/or EPROM with additional option;
external memory	64 x 2^{10} (16 bits wide), RAM and/or EPROM for data blocks
Operation set	Complete STEP 5 operation set (see Section 1.7)

Power supply unit

Input

Nominal AC voltage input V_{NI}	110 or 220 V ±15 % (Note: voltage selector switch)
Undervoltage signal	at $V_I \leq 187$ V
Input frequency f_I	50 Hz
Input current I_{NI} at 220 V (110 V) and rated load	2.95 A (5.9 A)
Inrush current i	200 A (100 A)
Efficiency at rated load	79 % without fan 65 % with fan

1) The processing time of operating system software (approx. 1.5 ms) must be added per program scan

2) 5 % arithmetic operations; 25 % load and transfer operations; 10 % jumps; 60 % binary operations

3) An additional 2112 inputs bytes and 2112 output bytes can be addressed if the 302 expansion unit interface module is used.

Back-up time on power failure	10 ms (typical)
Line-side fuse	6 A (quick response)

Output 1

DC output voltage V_{NO}	5.1 V ±0.5 %
Overvoltage shutdown	at V_O = 6 V ±5 %
Nominal output current I_{NO}	40 A
Overcurrent protection by current limiting	$\leq 1.05 \times I_{NO} < I_{NO} < 1.15 \times I_{NO}$
Ripple	$\leq$ 1 % of V_O
Dynamic voltage tolerances of V_O	
at load surge from 50 to 100 % I_N	$\leq$ 5 %
Settling time	$\leq$ 5 ms

Output 2

Nominal DC output voltage V_{NO}	24 V +25 %/-15 %
Output current I_{NO}	2.8 A
Total current load 24 V DC and 15 V DC output	$\leq$ 2.8 A
Overcurrent protection by fuse	$1.9 \times I_{NO}$
Ripple	$\leq$ 0.5 % of V_O

Output 3 (if additional module is retrofitted)

Nominal DC output voltage V_{NO}	15 V ±5 %
Nominal output current I_{NO}	2 A
Overcurrent protection via current limiting	$\geq$ 2 A
Overvoltage protection by short-circuiting the output	17.5 V ±3 %
Undervoltage indication by green LED on the frontplate	at 14 V ±3 %
Ripple	$\leq$ 5 % of V_{NO}

Fans

Number of fans	2
Operating voltage	110/220 V AC switch selectable
Volume flow per fan (acc. to data sheet)	160 m^3/h (5650 cu.ft./h)
Fan monitoring	Air flow monitoring with PTC thermistor as sensor; fan standstill is recognized and either 1. an LED lights up or a relay responds or 2. the output voltage is switched off

Backup battery

Type	Lithium primary cell
Capacity	5 Ah
Voltage	3.4 V
Backup time for maximum configuration	approx. 6 months with uninterrupted backup
Life	approx. 10 years without discharge

Caution! The backup battery contains lithium (≥ 0.5 g). Special transport regulations must be observed.

2 Installation

2.1 Installing the central controller

The S5-150 U central controller is designed for installation in cabinets, open racks or control desks.

M6 screws with washers must be used.

A clearance of at least 88.9 mm or 3 1/2 in. (2 U) must be left above, below and to the rear of the unit to permit the free flow of air.

The heat produced within the cabinet must be dissipated either by convection or forced ventilation.

2.2 Notes on installation

The line-side power supply cable must be kept as far away as possible from the other cables.

The 0V reference potential connection from the line-side power supply unit to the housing must be via a short, large-cross-section conductor (cross-section at least 10 mm^2) and laid separately from the signal leads.

The programmable controllers are supplied for operation with grounded reference potential.

If the programmable controller is installed in a cabinet, ensure a good metallic connection between the housing and the cabinet vertical members.

The load power supply must be installed at the top of the cabinet.

The 24 V DC load power supply must have smoothing capacitors (approx. 200 uF per ampere of load current). In addition, the transformer should have a shield winding.

The metallic parts of the cabinet (sides, door etc.) must be connected to each other through a low resistance connection (10 to 16 mm^2 conductor cross-section). The cabinet must be connected to the protective earth conductor.

If input/output cables are shielded they must be connected with cable clips to a shielding bar with a low-resistance connection to the programmable controller housing.

Inductive voltage spikes are limited on the output modules. To increase the immunity to noise, it is advisable nevertheless to fit the coils and contactors to be controlled with arc quenching elements (e.g. diode 1 N 4004).

If contactors are installed in the same cabinet as the programmable controller or in the vicinity of the cabinet, it is advisable to fit the contactor coils with RC elements (0.25 µF).

2.3 Connecting the cables

The connecting cables for programmer interface modules, expansion unit interface modules, interface modules for standard I/Os and test panel are connected via front connectors. The front connectors must be locked onto the front of the module by sliding the metal lever. Make sure that the correct front connectors are connected to the modules, as there is otherwise a danger of module destruction.

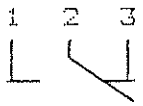
2.4 Connecting the power supplies

- Line connection
  Front terminals suitable for conductor cross-section up to 4 mm^2 (AWG 12) (L1, L2)
  Protective earth terminal with two M4 screw connections

- 24 V DC load voltage monitoring input
  Front terminals suitable for conductor cross-section up to 4 mm^2 (AWG 12)

- FRG/U_H
  Front terminals suitable for conductor cross-section up to 4 mm^2 (AWG 12)

- Relay signalling 1, 2, 3
  Front terminals suitable for conductor cross-section up to 4 mm^2 (AWG 12)



3 Operation

3.1 Notes

The supply voltage selected must be the same as that set on the internal switches (S10, S11; note markings printed on the electronics board). On the S10 ans S11 and on the frontplate the markings for the voltage not used must be covered.

No voltage exceeding 50 V may occur between the output terminals and the protective earth (PE).

The protective earth conductor must always be connected .

The power supply unit may only be withdrawn after the power cable has been disconnected.

If an overvoltage occurs at an output, the programmable controller is latched off (output voltage exceeded by $\leq$ 0.5 V). By switching the power supply off and on again, the power supply unit can once more be taken into operation provided the overvoltage was not caused by an internal fault.

Fault-free functioning is only guaranteed (power up 24 V DC part, fan monitoring) if the +5 V DC side has a minimal load of 1 A.

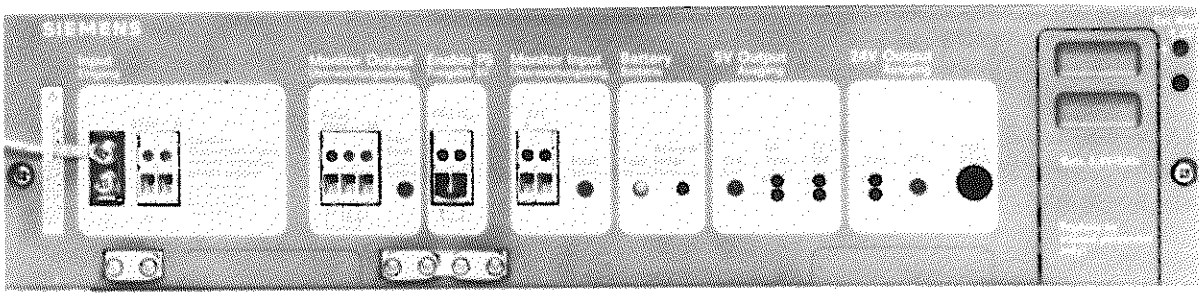
One U_H output (front terminal) must not be used for more than seven FRG inputs (front terminals).

An air filter can be inserted in the bottom of the power supply unit.

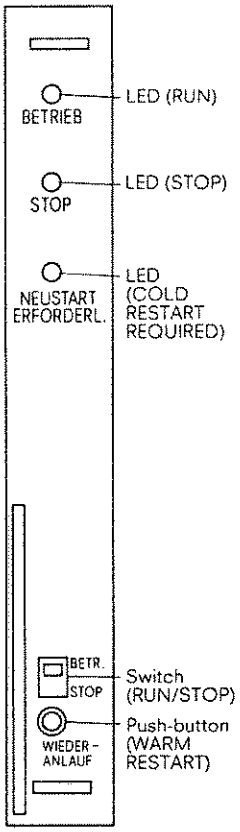
If an external battery is connected make sure that the voltage (3.4 V) and polarity are correct.

3.2 Controls and displays

3.2.1 Power supply unit with fan



3.2.2 The 926 CPU



- "RUN" LED
The LED indicates cyclic programm processing.

- "STOP" LED
The LED indicates that the programmable controller is in the stop state.

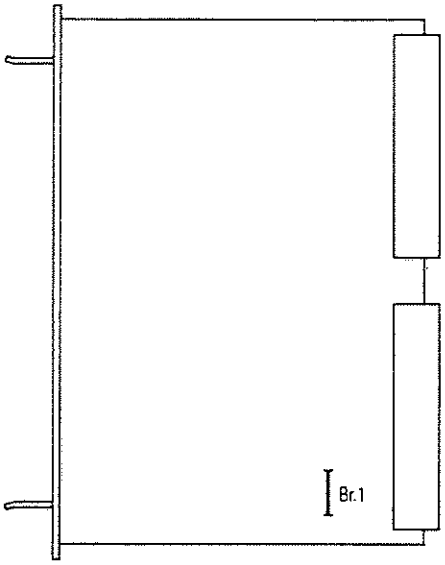
- "COLD-RESTART REQUIRED" LED
The LED indicates that a cold restart is required. A warm restart is not possible.

- "RUN/STOP"switch
The CPU enters the stop state after switching over from "RUN" to "STOP". In this case, the BASP signal is outputted in order to disable the I/Os.
When in the stop/state, the programmable controller has the DMA capacibility, the force on/off function is possible via the programming unit and, in addition, processing of a time interrupt is possible.
A cold restart is executed by the CPU after switching over from "STOP" to "RUN".

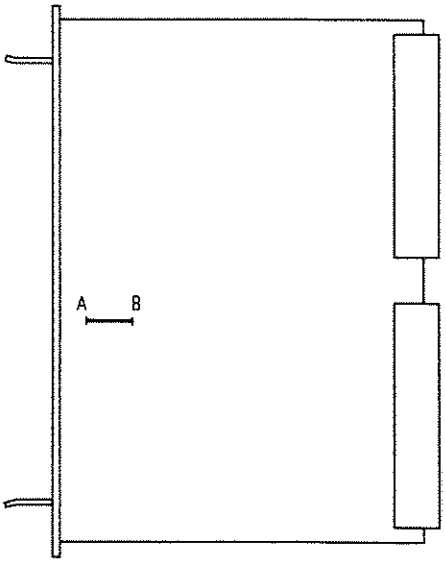
- "WARM RESTART" push-button
A warm restart is executed by the CPU when the pushbutton is actuated and the switch is simultaneously from "STOP" to "RUN".

3.3 Jumper assignments

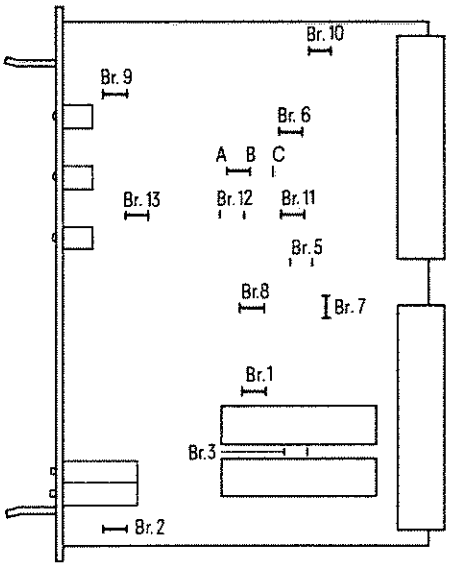
3.3.1 CPU modules



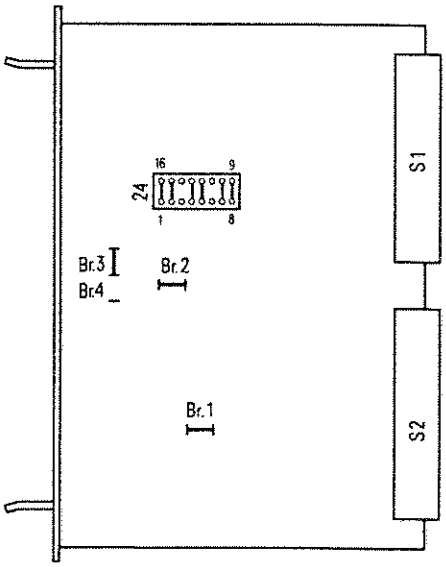
6ES5 924-3SA11



6ES5 925-3SA11



6ES5 926-3SA11



6ES5 927-3SA11

The standard jumper assignment is shown.

● CPU module 926

Jumper	inserted	open
Br. 5	**No** BASP is generated by test panel function (TE/BE).	BASP is generated by test panel function (TE/BE).
Br. 11	Cycle indication enabled.	Cycle indication disabled.
Br. 13	No automatic internal Ready generation of the CPU for time-out (QVZ) in single-step mode with the test panel, and thus no QVZ detection.	CPU reaction to QVZ and Ready in single-step mode as in normal operation.

– Time interrupt selection

Function	Jumpers
100 ms	Jumper A-B inserted Jumper B-C open
10 ms	Jumper A-B open Jumper B-C inserted
No time interrupt	Jumper A-B open Jumper B-C open

● CPU module 927

Jumper	inserted	open
Br. 1	Timers are up-dated.	Timers are not up-dated.

3.3.2 Power supply unit

Function	Jumpers
Battery monitoring (BAU) on Battery monitoring (BAU) off	NN–MM inserted [1] NN–MM open
Switching off the power supply after fan failure Without switching power supply off after fan failure (only indication via LED, relay)	F–R inserted [1] F–R open
Operation with load voltage monitoring Operation without load voltage monitoring	BA–EX open [1] BA–EX inserted
Driving the signalling relay (relay contact 2–3 closed) via RLSA without RLSA via BASPA (V_0 < 4.75 V or load voltage monitoring < 20 V – 25 %) without BASPA If neither jumper is inserted, the relay is only operated by the fan monitoring.	 RR–LL inserted RR–LL open [1] BB–AA inserted BB–AA open [1]

[1] As supplied.

Fan failure, RLSA or BASPA relay signal

Fault		Signal		Output voltages switched off	
		LED	Relay contact	F–R open	F–R inserted [1]
Fan failure		bright	2–3 closed	no	yes
and RLSA = LOW		bright	2–3 closed	no	yes
or BASPA = LOW		bright	2–3 closed	no	yes
Fan o.k.		dark	2–1 closed	no	no
and RLSA = LOW		dark	2–3 closed	no	no
or BASPA = LOW		dark	2–3 closed	no	no
Enable missing	BB–AA open	dark	2–1 closed	yes	yes
	BB–AA closed	dark	2–3 closed	yes	yes
U_H–FRG open	RR–LL closed RLSA = LOW	dark	2–3 closed	yes	yes

[1] As supplied.

3.3.3 Wiring backplane

	Signal	Slots 139 and 147 for AS 301 EU interface module (as supplied)	for CP 5xx
Jumper 1	UBAT	open	inserted
Jumper 2	+24 V	open	inserted
Jumper 3	+15 V	open	inserted
Jumper 4	M2	open	inserted
Jumper 5	DSI	open	inserted
Jumper 7	NAU	open	inserted
Jumper 8	BAU	open	inserted

	Signal	Slot 107 for CP 5xx, 302, memory	for parity module
Jumper 9	PARI	open	inserted

	Signal	Slot 115 for CP 5xx, 302, memory	for parity module
Jumper 10	PARI	open	inserted

	Signal	Slot 3 [1] for memory	for parity module
Jumper 11	PARI	open	inserted

Note: Inserting modules into slots configured for other modules normally causes those or other modules to be destroyed.

3.4 Start-up

- Line voltage

The PC is set for operation on 220 V. The frontplate is labelled accordingly. If the customer wishes to operate it on 110 V (115 V), the power supply unit must be removed and set to 110 V with the sliding switches. Before re-inserting the power supply, the 110 V label must be stuck over the 220 V inscription. When installing the power supply unit, take care to connect the short protective earth connection cable to the power supply unit and housing.

- Slot configuration:

The labelling strip in the top locking bar gives the possible configurations for both variants.

To simplify start-up and servicing, the configuration used should be marked. The variant not set should be covered with a small white label (supplied).

- The backup battery is supplied loose and must be inserted before start-up. Without a backup battery the PC remains in the STOP state after the power has been switched on.

- A 340 or 350 memory module must be inserted before start-up. The operating system reserves an area of 1102 words in the RAM from address 56×2^{10} downwards for the block address list.

[1] If external memory interface module is in slot 27.

It must be noted that EPROMs are addressed in ascending order from 8×2^{10} (2000 H) upwards and RAMs in descending order from 56×2^{10} (OE00H) downwards.

- The power supply unit only switches on the +5 V supply if both fans have reached a sufficient speed.

- The cable jumper from U_H to FRG at ENABLE PS enables the power supply unit. By linking several power supply units via the monitoring outputs and the enable inputs, these can be disabled together in the case of a fault.

- Undervoltage or no voltage on the monitor input for 24 V DC triggers the BASP signal in the PC and in the connected expansion units, causing all digital outputs to be disabled. The central processing units do not react.

4 Maintenance

4.1 General

In the central controller, modules must never be inserted or pulled out under power.

The power supply unit must not be removed under power.

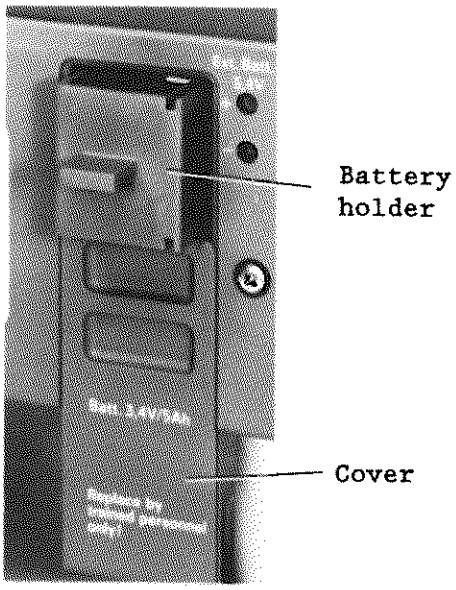
4.2 Replacing the backup battery

The backup battery can be changed without the memory contents being lost if the power supply unit remains on and/or an external 3.4 V voltage is applied to the "Ext. Batt" terminals.

The backup battery must be replaced at least every 3 years (available capacity: 5 Ah).

- Slide cover down
- Pull out battery holder
- Change battery

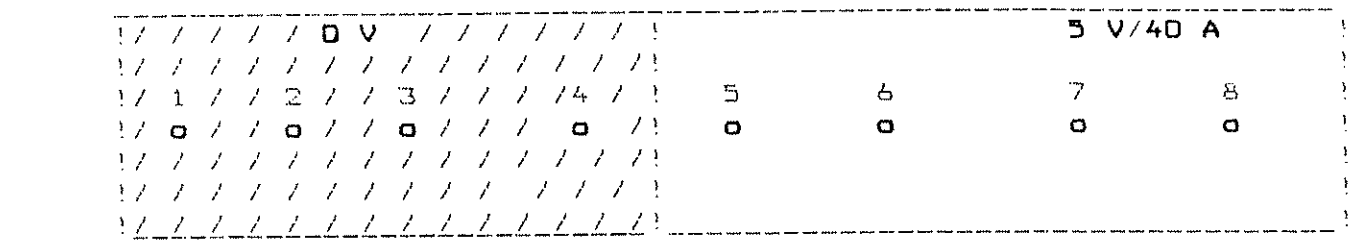
Apart from this, the power supply unit needs no maintenance.



4.3 Interface assignments

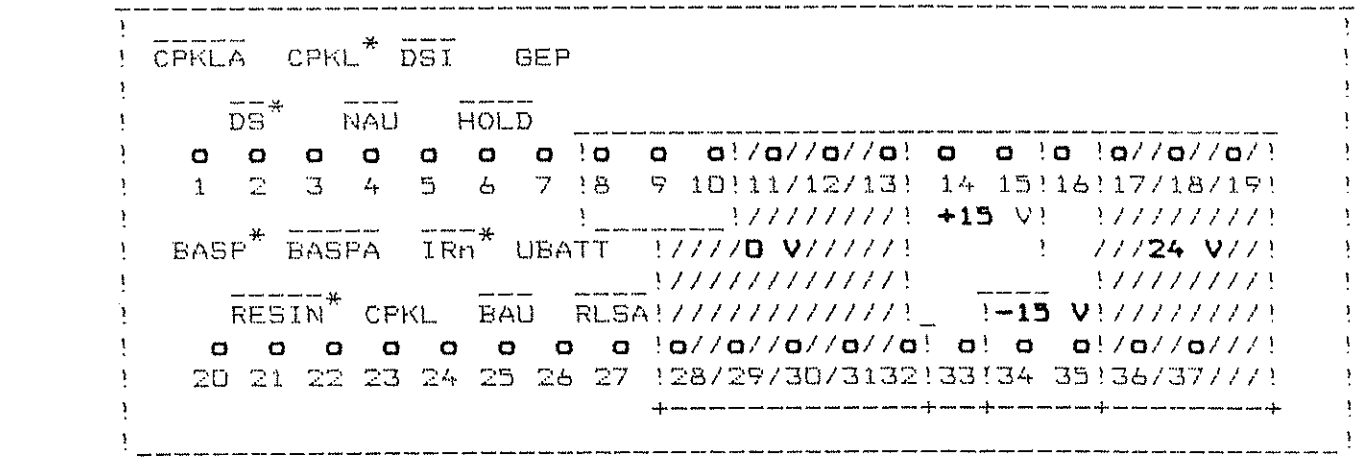
Power connections:
Subminitiature connector, 8-pole, with 5 high current contacts,
type D to MIL-C24308

Connector X1 seen from the rear:



Signal connections:
Subminiature terminal block 37-pole, type D to MIL-C24308

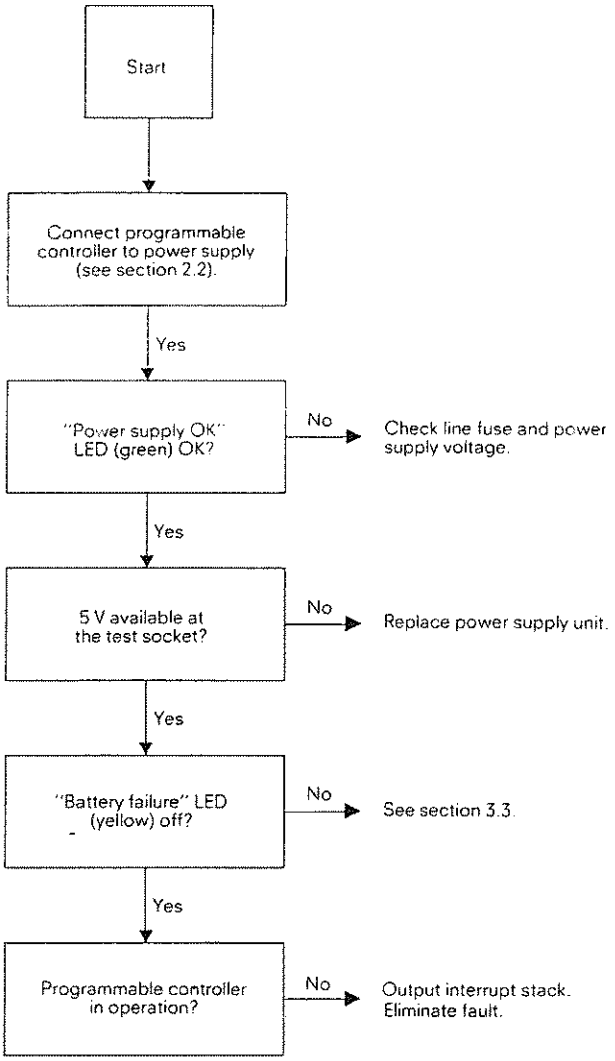
Connector X2, seen from the rear:



* MC 210 application

4.4 Repair

Flow chart
The flowchart below is only a recommendation. A detailed trouble-shooting specification is not possible owing to the multiple signal paths. Refer to page 4 for the principle of operation of the central processor.



4.5 Control bits and interrupt stack

CONTROL BITS

```
ENDSCH  PBSSCH  BSTSCH  SCHTAE  ADRBAU  SPABBR  NAUAS   QUITT

EXSPVH  NSTPAN    NB      NB    PFEANW  PFESYS  PBEXSP  PBHSP
  X       X                                       X

STOZUS  STOANZ  NEUSTA  WIEDAN  BATPUF  DATEIN   BARB   BARBEND
  X       X               X       X
  NB    UAFEHL  MAFEHL    EOVH   MANAU  WWAKT   OBWIED  OBNAU
                            X               X

TESBST  QVZNIO  KOPFNI  PROEND  WECKFE  PADRFE  ASPLUE  RAMADFE

  NB    SYNFEH  NINEU   NIWIED  RUFBST  QVZNIN   SUMF   URLAD

 STPA   TSBUNT    NB      NB    TBWFEH  LIRTIR  WASTOP  WIEEND

LUECK     NB    DATANF  UEBF    UESYS  WECKAK  PROMEI  QVZTES
```

```
*COMMAND*  HARDCOPY
CALL     'STACK'
```

INTERRUPT STACK

```
DEPTH:    01

INS-REG:  CD64      SAC:       A49E      DB-ADD:   0000      BA-ADD:   0E6E
BLK-STP:  EBA9      PB-NO.:       1      DB-NO.:             OB-NO.:     43
                    REL-SAC:   0001      DBL-REG:  0000
VEC-ADD:  0000      UAMK:      0040      UALW:     FFFF

ACCU1: 0000 0040    ACCU2: 0000 0040    ACCU3: 0001 0E3C    ACCU4: 0000 0000


RESULT BITS:        FLG1 FLG0 OVFL OVFLS OR   STATUS RLO FC0P
                     X                         X      X   X

CAUSE OF INTERR.:   STOPS STUEB NAU QVZ ZYK BAU SUF STUEU ADF PARI TRAF
                                                          X
```

```
*COMMAND*  HARDCOPY
CALL     'STACK'
```

ENDSCH	Shift block to end
PBSSCH	Block shift
SCHTAE	Shifting in progress
SPABBR	Memory shift abort
EXSPVH	Peripheral memory available
PFEANW	Parity error in user memory
PFESYS	Parity error in system program
PBEXSP	Parity error module, peripheral memory
PBHSP	Parity error module, main memory
STOZUS	PC stopped
NEUSTA	PC enters cycle by cold restart
WIEDAN	PC enters cycle by warm restart
BATPUF	Power supply has battery backup (operation without backup not permissible)
DATEIN	Contents of data and time-of-day locations not valid for time interrupt
BARB	Program check
MAFEHL	Indentifier indicating that an entry has been made in the machine error word
EOVH	Process interface module EO plugged in
MANAU	Warm restart after power failure
OBWIED	User OB 21 being processed or not yet terminated
OBNAU	User OB 22 being processed or not yet terminated
TESBST	Test block not OK
KOPFNI	Block header cannot be interpreted
PROEND	Shifting terminated before plugging in PROM
WECKFE	Time interrupt processing error (time interrupt has interrupted itself)
PADRFE	Addressing error in user PROM
ASPLUE	User memory has addressing gaps
RAMADFE	Addressing error in user RAM
SYNFE	Synchronization error in user memory (illegal code)
NINEU	Cold restart not possible (IPL necessary)
NIWIED	Warm restart not possible (cold restart necessary)
RUFBST	Call for a non-existent block
SUMF	Sum check error (replacement of system program memory)
URLAD	Initial program loading, i.e. general reset necessary
WASTOP	Warm restart if stop switch also actuated
LUECK	Gap between blocks in RAM
DATANF	Prompt to entry current date and time-of-day
WECKAK	Time interrupt processing not active
INS-REG	Statement register
BLK-STP	Block stack pointer
VEC-ADD	Vector address for external memory
SAC	Step address counter status
PB-NO	Current block whose processing has caused the interruption
REL-SAC	Relative step address counter status in current block
UAMK	Interrupt condition code mask
DB-ADD	Data block starting address
DB-NO	Current data block
DBL-REG	Register containing the length of data block
UALW	Interrupt condition code
BA-ADD	Block starting address
OB-NO	Block from which the current block is called
STOPS	Stop switch
STUEB	Block stack overflow
NAU	Power failure
QVZ	Time-out (acknowledgment delay)
ZYK	Cycle time exceeded
BAU	Battery low
SUF	Substitution error
STUEU	Interrupt stack overflow
ADF	Addressing error
PARI	Parity error
TRAF	Transfer error

5 Spare parts

Power supply unit with fan	6ES5955-3LF11
Backup battery	W79084-L1001-B5
Battery holder	6XW79084-L1001-B5
CPU 1	6ES5924-3SA11
CPU 2	6ES5925-3SA11
CPU 3	6ES5926-3SA11
CPU 4	6ES5927-3SA11
Jumpering card	6ES5756-0AA11

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